



**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application.

**Listing of Claims:**

Claim 1 (currently amended): A static logic circuit on a SOI substrate, comprising:

a pull-up network comprising a plurality of parallel connected MOS transistors with a first and second common node, wherein at least one of said plurality of parallel connected MOS transistors is a NMOS transistor and at least one of said plurality of parallel connected MOS transistors is a PMOS transistor;

a circuit supply voltage which is connected to said first common node of said pull-up network;

a pull-down network which is connected to said second common node of said pull-up network wherein said pull-down network comprises a plurality of series connected MOS transistors connected to a circuit ground; and

an output node which is connected to said second common node of said pull-up network.

Claim 2 (canceled)

Claim 3 (currently amended): The static logic circuit of claim 2 1 wherein at least one of said plurality of series connected MOS transistors is a NMOS transistor and at least one of said plurality of series connected MOS transistors is a PMOS transistor.

Claim 4 (original): The static logic circuit of claim 1 wherein at least one of said MOS transistors in said pull-up network has a gate tied to a floating substrate body.

Claim 5 (currently amended): The static logic circuit of claim 2 1 wherein at least one of said MOS transistors in said pull-down network has a gate tied to a floating substrate body.

Claim 6 (currently amended): A static logic circuit on a SOI substrate, comprising:

a pull-down network comprising a plurality of parallel connected MOS transistors with a first and second common node, wherein at least one of said plurality of parallel connected MOS transistors is a NMOS transistor and at least one of said plurality of parallel connected MOS transistors is a PMOS transistor;

a circuit ground which is connected to said first common node of said pull-down network;

a pull-up network which is connected to said second common node of said pull-down network wherein said pull-up network comprises a plurality of series connected MOS transistors connected to a circuit supply voltage; and

an output node which is connected to said second common node of said pull-down network.

Claim 7 (canceled):

Claim 8 (currently amended): The static logic circuit of claim 7 6 wherein at least one of said plurality of series connected MOS transistors is a NMOS transistor and at least one of said plurality of series connected MOS transistors is a PMOS transistor.

Claim 9 (original): The static logic circuit of claim 6 wherein at least one of said MOS transistors in said pull-down network has a gate tied to a floating substrate body.

Claim 10 (currently amended): The static logic circuit of claim 7 6 wherein at least one of said MOS transistors in said pull-up network has a gate tied to a floating substrate body.

Claim 11 (original): A static logic circuit on a SOI substrate, comprising:

- a pull-down network comprising a plurality of parallel connected PMOS transistors with a first and second common node;

- a circuit ground which is connected to said first common node of said pull-down network;

- a pull-up network which is connected to said second common node of said pull-down network; and

- an output node which is connected to said second common node of said pull-down network.

Claim 12 (original): The static logic circuit of claim 11 wherein said pull-up network comprises a plurality of series connected NMOS transistors connected to a circuit supply voltage.

Claim 13 (original): The static logic circuit of claim 11 wherein at least one of said MOS transistors in said pull-down network has a gate tied to a floating substrate body.

Claim 14 (original): The static logic circuit of claim 12 wherein at least one of said MOS transistors in said pull-up network has a gate tied to a floating substrate body.

Claim 15 (original): A static logic circuit on a SOI substrate, comprising:

a pull-up network comprising a plurality of parallel connected NMOS transistors with a first and second common node;

a circuit supply voltage which is connected to said first common node of said pull-up network;

a pull-down network which is connected to said second common node of said pull-up network; and

an output node which is connected to said second common node of said pull-up network.

Claim 16 (original): The static logic circuit of claim 15 wherein said pull-down network comprises a plurality of series connected PMOS transistors connected to a circuit ground.

Claim 17 (original): The static logic circuit of claim 15 wherein at least one of said MOS transistors in said pull-up network has a gate tied to a floating substrate body.

Claim 18 (original): The static logic circuit of claim 16 wherein at least one of said MOS transistors in said pull-down network has a gate tied to a floating substrate body.